UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,552	04/02/2004	Mirsaid Bolorforosh	2004P03346US	2523

7590 06/13/2007

Siemens Corporation
Intellectual Property Department
170 Wood Avenue South
Iselin, NJ 08830

EXAMINER	
KITOV, ZEEV V	
ART UNIT	PAPER NUMBER
2836	

MAIL DATE	DELIVERY MODE
06/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,552	BOLORFOROSH ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 6, 9 - 16, 18, 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 6, 9 - 16, 18, 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on May 8, 2007. Claims 1, 2 and 12 are amended. A new search revealed new evidence. Accordingly the finality of the last Office Action is withdrawn. A new Office Action follows.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baumgartner et al. (US 2004/0113524) in view of Amano (US 7,032,454) and Hogg (US 7,046,488). Regarding Claim 1 Baumgartner et al. disclose the capacitive membrane ultrasound transducer (Fig. 1) including a flexible membrane (8 and 12 in Fig. 1) adjacent a void (20 in Fig. 1). It inherently includes a conductor connected with the flexible membrane, since otherwise the transducer cannot function. However, it does not disclose a voltage limiting circuit. Amano teaches that the capacitive membrane is vulnerable to the high voltages (ESD prone, col. 1, lines 62 – 64). Therefore, one of ordinary skill in the art would realize necessity of protecting the capacitive membranes against over-voltages.

Hogg discloses the switch protecting the over-voltage sensitive element, disk drive head, against over-voltages (Fig. 2 and 3, col. 4, line 21 – col. 5, line 22). The switch in form of a voltage clamping MOS transistors protects the head (18 in Fig. 3) by shorting it while the head is not being used. According to McGraw-Hill Dictionary of Scientific and Technical Terms (page 1783), a relay is defined as "a device that is operated by a variation in the conditions in one electric circuit and serves to make or break one or more connections in the same or another electric circuit". The Hogg's switch clearly fits this definition, since it is a device operated by a change in conditions in one electric circuit, i.e. closing or opening switch 34 in Fig. 3, thus causing a make or break, switching on/off transistors 26C, 26B and 26A in Fig. 3. The reference is pertinent to the problem solved by the inventor, i.e. protection of the over-voltage sensitive elements against ESD. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Baumgartner et al. solution by adding the voltage limiting circuit according to teachings of Hogg, because according to Hogg (col. 1, lines 24 – 28), the ESD can damage the over-voltage-sensitive element while inactive, such as during manufacturing or while the circuit is powered down or while the element is not used during normal operation of the system.

Regarding Claim 2, Baumgartner et al. disclose the conductor including an electrode on the flexible membrane (12 in Fig. 1) and inherently a signal trace connected with the electrode, since otherwise the device is inoperative. Since the electrode is located on the top of the flexible membrane an alternative way, i.e.

connecting the electrode by any other structure, such as a common ground plate is impossible.

Regarding Claims 9 and 10, Hogg discloses the protection circuit being integrated within a preamplifier (Fig. 4) and within a transducer probe (Fig. 6B). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Baumgartner et al. solution by integrating the protection circuit within a preamplifier and within a transducer probe according to teachings of Hogg, because (a) such integration will bring well known in the art advantages such as miniaturization and improvement in reliability, and (b) according to Court Decision *In re Larson,* 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965) "the use of a one piece construction instead of the structure disclosed in the prior art would be merely a matter of obvious engineering choice."

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baumgartner et al. in view of Amano, Hogg and Baxter et al. (US 5,407,854). As per Claim 3, it differs from Claim 1 rejected above by its limitation of zener diodes used as over-voltage protecting element. Hogg discloses shorting the protected element inputs (29A and 20B in Fig. 3) to the ground. Baxter et al. disclose protecting the ion sensor against over-voltages by including zener diodes connected across the input sensor interface capacitor (201 in Fig. 2). In the Baumgartner et al. circuit modified according to teachings of Hogg and Baxter et al. the zener diodes are connected between one of the terminals and the ground. The reference has the same problem solving area, namely

providing an over-voltage protection for the capacitive sensor. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Baumgartner et al. solution by adding the zener diodes connected between one of the electrodes of the capacitive transducer and the ground, because as Baxter et al. state (col. 2, lines 17 – 22), the zener diodes are necessary to protect the circuit against ESD damage.

Regarding Claim 4, Baxter et al. disclose two zener diodes connected in series with opposite polarities (Fig. 2). A motivation for modification of the primary reference is the same as above.

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baumgartner et al. in view of Amano, Hogg and Horowitz et al. textbook The Art of Electronics. As per Claim 5, it differs from Claim 1 rejected above by its limitation of the limiting circuit including diodes biased by a voltage source. Horowitz et al. disclose the diode clamping, i.e. voltage limiting circuits including diodes biased by the voltage sources (Fig. 1.84 - 1.86, page 49 – page 50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Baumgartner et al. solution by adding the voltage limiting circuit including the diodes biased by the voltage source according to teachings of Horowitz et al., because as Horowitz et al. state (page 49, last paragraph – page 50, 1st paragraph), such diode clamps is standard equipment on all inputs in the CMOS family, since without them the

delicate input circuits are easily destroyed by static electricity discharges during handling.

As per Claim 6 it differs from Claim 5 by its limitation of the second diode biased by a negative voltage. The second diode performs the same function as the first diode; the only difference is in the polarity of the voltage source. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Baumgartner et al. solution by adding the second diode biased by the negative polarity voltage source in the same manner as the first diode, because According to Court Decision *In re Harza,* 274 F.2d 669, 124 USPQ 378 (CCPA 1960); the court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baumgartner et al. in view of Amano, Hogg and Nakamura (US 5,225,958). As per Claim 11, Baumgartner et al., Amano and Hogg disclose all the elements of Claims 1. However, regarding Claim 11, they do no not disclose at least one element of the voltage limiting circuit being positioned within a transducer connector. Nakamura discloses a microswitch (90 in Fig. 16), which is a component of the over-voltage protecting circuit (col. 8, lines 33 – 67) being positioned within a connector (12D in Fig. 16) of the solid-state image sensor. The reference has the same problem solving area, namely providing an over-voltage protection for the voltage sensitive sensors. It would have been obvious to one of ordinary skill in the art at the time the invention was made

to have modified the Baumgartner et al. solution by integrating the microswitch according to teachings of Nakamura within the connector, because as Nakamura states (col. 8, lines 33 – 67), such arrangement will make sure proper functioning of the over-voltage protection circuitry.

Claims 12 – 14, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baumgartner et al. (US 2004/0113524) in view of Amano (US 7,032,454) and Hogg (US 7,046,488). Regarding Claim 12, Baumgartner et al. disclose the capacitive membrane ultrasound transducer (Fig. 1) including a flexible membrane (8 and 12 in Fig. 1) adjacent a void (20 in Fig. 1). It inherently includes a conductor connected with the flexible membrane, since otherwise the transducer cannot function. It further discloses the membrane generating either acoustic or electric signal (paragraphs [0002] - [0007]). However, it does not disclose a voltage limiting circuit. Amano teaches that the capacitive membrane is vulnerable to the high voltages (ESD prone, col. 1, lines 62 – 64). Therefore, one of ordinary skill in the art would realize necessity of protecting the capacitive membranes against over-voltages.

However, none of the references discloses limiting a voltage across the protected element at a time other than during performance. Hogg discloses the voltage limiting circuit protecting the over-voltage sensitive disk drive head against over-voltages (Fig. 2 and 3, col. 4, line 21 – col. 5, line 22). The voltage limiting depletion-type MOS transistors (24C, 24B and 24 A in Fig. 3) protect the head (18 in Fig. 3) by shorting it while the head is not being used. The reference is pertinent to the problem solved by

the inventor, i.e. protection of the over-voltage sensitive elements against ESD. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Baumgartner et al. solution by adding the voltage limiting circuit according to teachings of Hogg, because according to Hogg (col. 1, lines 24 – 28), the ESD can damage the over-voltage-sensitive element while inactive, such as during manufacturing or while the circuit is powered down or while the element is not used during normal operation of the system.

Regarding Claims 13 and 14, Hogg discloses the protection circuit (Fig. 3), shorting and thus holding the voltage constant (equal zero) across the protected element and draining current away from the protected element at the time while the power is down and the voltage (such as ESD) exceeds a breakdown voltage of the protected element (col. 4, line 65 – col. 5, line 4). Alternatively, a prior art in the Hogg reference (Fig. 1) demonstrates a protection circuit holding a constant voltage and draining current away from the protected element. A motivation for modification of the primary reference is the same as above.

Regarding Claims 18 and 19, Hogg discloses the protection circuit being integrated within a preamplifier (Fig. 4) and within a transducer probe (Fig. 6B). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Baumgartner et al. solution by integrating the protection circuit within a preamplifier and within a transducer probe according to teachings of Hogg, because (a) such integration will bring well known in the art advantages such as miniaturization and improvement in reliability, and (b) according to Court Decision *In re*

Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965) "the use of a one piece construction instead of the structure disclosed in the prior art would be merely a matter of obvious engineering choice."

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baumgartner et al. in view of Amano, Hogg and Baxter et al. (US 5,407,854). As per Claim 15, it differs from Claim 12 rejected above by its limitation of zener diodes used as over-voltage protecting element. Hogg discloses shorting the protected element inputs (29A and 20B in Fig. 3) to the ground. Baxter et al. disclose protecting the ion sensor against over-voltages by including zener diodes connected across the input sensor interface capacitor (201 in Fig. 2). In the Baumgartner et al. circuit modified according to teachings of Hogg and Baxter et al. the zener diodes are connected between one of the terminals and the ground. The reference has the same problem solving area, namely providing an over-voltage protection for the capacitive sensor. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Baumgartner et al. solution by adding the zener diodes connected between one of the electrodes of the capacitive transducer and the ground, because as Baxter et al. state (col. 2, lines 17 – 22), the zener diodes are necessary to protect the circuit against ESD damage.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baumgartner et al. in view of Amano, Hogg and Horowitz et al. textbook The Art of Electronics. As per Claim 16, it differs from Claim 12 rejected above by its limitation of the limiting circuit including diodes biased by a voltage source. Horowitz et al. disclose the diode clamping, i.e. voltage limiting circuits including diodes biased by the voltage sources (Fig. 1.84 - 1.86, page 49 – page 50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Baumgartner et al. solution by adding the voltage limiting circuit including the diodes biased by the voltage source according to teachings of Horowitz et al., because as Horowitz et al. state (page 49, last paragraph – page 50, 1st paragraph), such diode clamps is standard equipment on all inputs in the CMOS family, since without them the delicate input circuits are easily destroyed by static electricity discharges during handling.

Response to Arguments

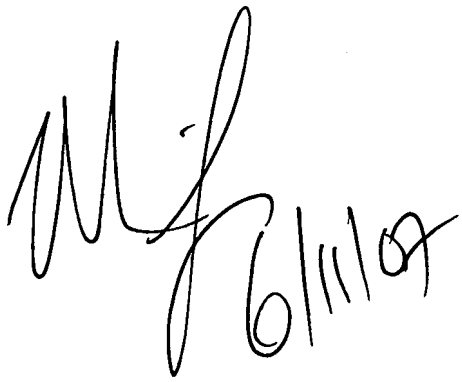
Applicant's Arguments have been given careful consideration but they are now moot in view of new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach

examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry, can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
6/11/2007



MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800